

INTRODUCTION

The WL102 execute mode is provided to allow processors that have separate read only code space from their read/write RAM space to perform in-system re-programming of their code space. This is achieved by re-mapping the code space to perform read cycles on the Buffer RAM of the WL102 whilst all write cycles cause a CCEB (Code Chip Enable) strobe. This allows the processor to execute code from the Buffer RAM and perform write cycles on the code memory area. A program can then be loaded into the buffer RAM by the Host which, when executed, reprograms the Flash code ROM. This also has the advantage that Flash memory can be erased and re-programmed without having to provide any other alternative code space during the operation.

When using the internal 8051, execute mode guarantees that the processor can always be recovered from any incorrect operation which causes corruption of code memory. The Flash ROM can also be programmed after board assembly, possibly during final test, since no bootstrap code is needed to perform in system programming. This allows test code to be loaded and also ensures that MAC software can be updated easily in the field or at the end of manufacture.

A set of Mitel utilities is available which perform Flash upgrading of the DE6038 system.

HARDWARE OPERATION WITH EXTERNAL PROCESSOR

In order to use this feature with an external processor it is necessary to provide signals which differentiate between Code space read cycles and other memory read cycles to the WL102. Code memory select should use the SPSENB input signal and normal memory read and write should use SRDB and SWRB. In normal running mode (non execute) the SPSENB input is buffered inside the WL102 and drives the CCEB signal, which is used to chip select the code ROM. In normal mode an SWRB cycle does not cause a CCEB output and so the SWRB signal can be tied to the Flash write enable pin. See Fig. 1.

When the WL102 is switched to execute mode the SPSENB input is used to cause a Buffer RAM read cycle (with no CCEB signal being generated) and the SWRB input causes CCEB to select the Flash ROM.

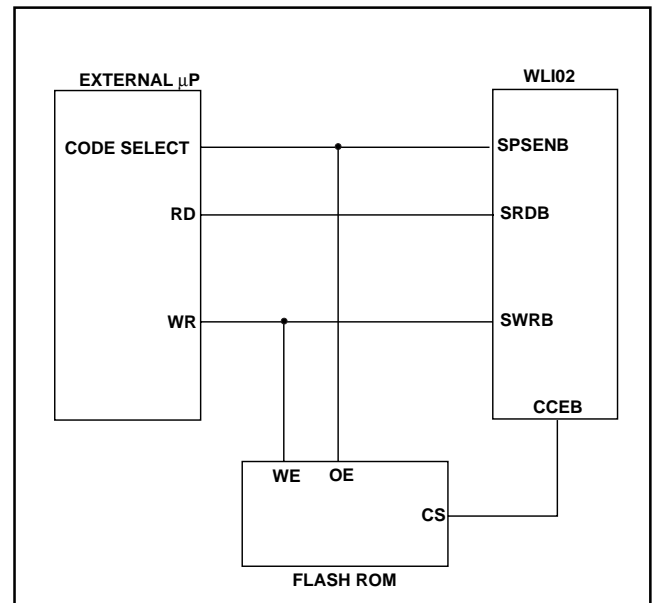


Fig. 1 External Hardware Requirements

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With an external 8051 the PSEN (Code ROM read) signal would be used as the code select in Fig. 1 and 8051's external memory read, p3[7], and write, p3[6], signals would be the SRDB and SWRB signals.

Butterfly

Using a GPS ARM™ Butterfly device as the external processor the Code Select signal would typically be the CS0 signal ORed with the OE signal (memory area 0 read). The memory peripheral controller would be set up for 8 bit accesses to this area with sufficient wait states for the speed of Flash ROM with the propagation delay of the WL102 CCEB signal included, since the Flash is selected by CCEB. It is important to note that the SPENB signal is a read strobe in itself and so no SRDB strobe should occur during a code read cycle. It is therefore also necessary that during normal operation this memory area is set to read only mode.

The SRDB and SWRB signals would be the OE and WE0 signals of the Butterfly. In order to prevent spurious reads and writes to the WL102 one of the CSx signals can be inverted and used as the MSB of the address bus. In this way only accesses to that memory block will fall within the address decode of the WL102.

HARDWARE OPERATION WITH INTERNAL 8051

When using the internal 8051 the necessary hardware connection are provided on chip.

EFFECT OF EXECUTE MODE ON WL102

The Host controls EXECUTE mode operation by setting the EXECUTE bit in the control register (Addr 0). When this bit is set a number of hardware changes occur in the WL102.

1. The entire address map is disabled. None of the blocks of the WL102 can be accessed by the system processor using the SRDB or SWRB signals. This is necessary to allow the MAC system processor to be able to write to any address location whilst programming the Flash ROM.
2. All SWRB cycles cause the CCEB output to become active. If the CCEB signal is tied to the Flash ROM chip select this effectively maps the entire address map to the Flash ROM device.
3. All SPSENB cycles cause a byte to be read from the Buffer RAM. This maps the entire code space of the memory map to the Buffer RAM. The significant limitation of this is that the Buffer RAM can only be read sequentially, i.e. the address bus has no effect on the data that is read.
4. The SPSENB signal no longer causes a CCEB chip select to the Flash ROM. This prevents the Flash from outputting data whilst instructions are being from the Buffer RAM.
5. The system Buffer RAM address increment control signal is overridden so that the buffer RAM address always increments on every SPSENB cycle.

Once the WL102 is in execute mode the MAC system processor can be taken out of reset and all subsequent instruction read cycles read a byte from the Buffer RAM. Since the Buffer RAM has a one cycle latency the first byte read will be the contents of the System data holding register. In order for this to be determinate the host sets and then clears the CLEAR bit of the control register. This resets the data holding register to zero and also sets the System buffer RAM address counter to zero. In this way the first instruction byte fetched will always be zero and from then on the contents of the Buffer RAM starting at address zero.

Due to the sequential read nature of the Buffer RAM and the fact that the first instruction byte will always be a zero it is then necessary to write the code with these limitations in mind.

SOFTWARE OPERATION

Once the WL102 is correctly connected to make use of execute mode, the next stage is to develop the software to perform a Flash upgrade.

Two pieces of software are required to perform the upgrade:

1. Host software to load the Buffer RAM and control execution of the Flash upgrade software.
2. System software which is loaded into the buffer RAM and executed in the system processor which actually performs the write cycles necessary to re-program the Flash ROM.

Host Software

The Host software required to perform a Flash upgrade must control the WL102 to perform the necessary functions to allow the System software to run from the Buffer RAM. The sequence required can be seen in Fig. 2.

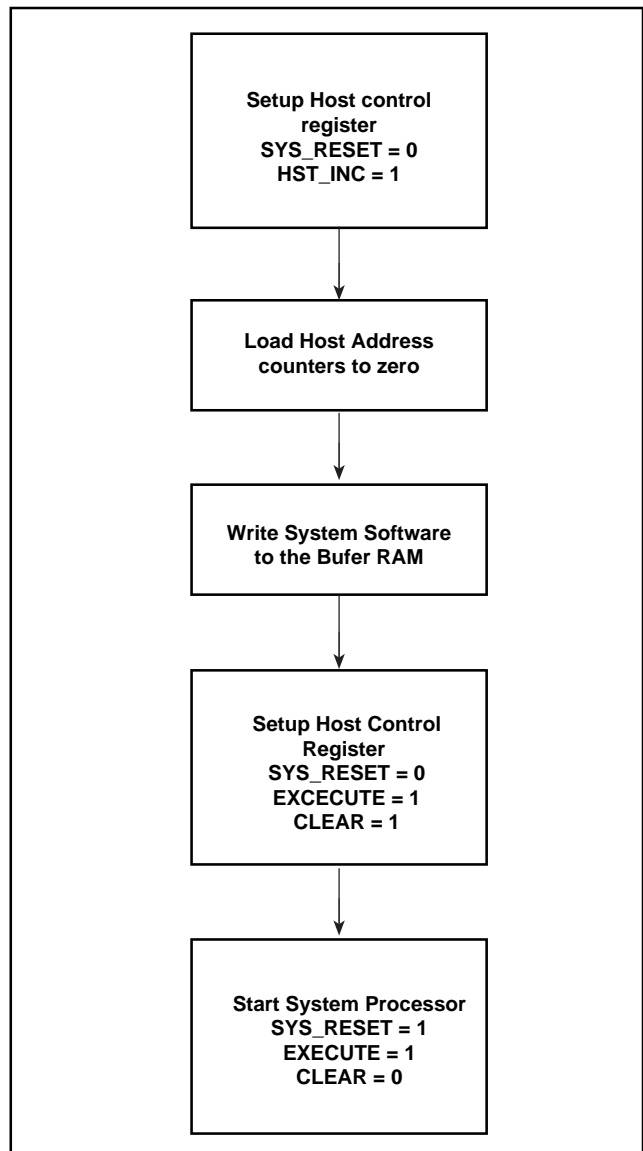


Fig. 2 Host Software Flowchart

Initially the MAC system processor is placed into reset and the Host switches its Auto-Increment bit on. The required software is then written to the Buffer RAM starting at Buffer RAM address 0, by writing it byte to byte to the Host data register. Once this is complete the Host performs a CLEAR operation which resets the MAC system Buffer RAM address registers and the data holding register. Finally the MAC system processor is taken out of reset and allowed to execute the code in the Buffer RAM by setting the EXECUTE bit in the Host control register.

System Software

The system software required to perform a Flash upgrade will vary from processor to processor and for different Flash memories. For the purpose of explanation the 8051 is considered.

The software should be written to perform the necessary writes to the Flash ROM to erase and then program the locations as necessary. Since the erase operation is usually quite long and also sector programming can be slow, it is usually necessary to break the code into sections so that one section can be run at a time, with the Host allowing each section to run and then waiting the required amount of time before loading the next section of code.

The writing of the code is simple enough until the limitations of the Buffer RAM are considered. These are that the first byte read will always be a zero and that bytes have to be read sequentially. The effect of the first byte being zero requires that this must be followed by bytes which make up a valid instruction for the processor being used.

For an 8051 the instruction 0x00 is a NOP. However since the 8051 always reads two bytes per instruction and a NOP is a single byte instruction it is necessary to pad the downloaded code with an additional NOP to restore the correct instruction boundary. The second restriction of sequential reading of the Buffer RAM necessitates further changes to the machine code to be run on the MAC processor. An example can be seen in Fig. 3.

The 8051 processor performs two PSEN, instruction read, cycles per instruction. In Fig. 3 the instruction INC A is read in the first PSEN cycle. This is a single byte instruction and so the second PSEN cycle in this instruction cycle is discarded. In normal operation the address bus would remain static between the discarded PSEN cycle and the next PSEN cycle. This would effectively mean that the next instructions first byte is read twice. Since the Buffer RAM presents data sequentially it is therefore necessary to load the buffer with this double reading of the instruction byte. For example if the code needed to increment the A register twice the following Op codes would have to be loaded:

- 0x04 INC A
- 0xXX Dummy byte (not used)
- 0x04 INC A
- 0xXX Dummy byte (not used)

A final limitation of this mode is that any jump instruction is effectively meaningless since the address bus is ignored. This also applies to conditional jumps and calls

UTILITIES AVAILABLE

Since the use of EXECUTE mode is quite complex GPS provide a set of utilities which perform Flash upgrading of a DE6038 system.

Host software is available for PC which will control the Flash upgrade process. This requires a PC-Card enabler to be loaded if the DE6038 is plugged into a PC-Card slot. The source code can be easily modified for access to the WL102 at any IO or memory address.

A further PC based program is available which will take a binary program file for the internal 8051 and pad it as necessary for it to successfully run from the Buffer RAM on the internal processor.

Finally two program hex files are available for programming AMD29F010 and SST29VE010 devices. These can be used with the PC host based software to perform a Flash upgrade on the reference PCMCIA DE5038 design.

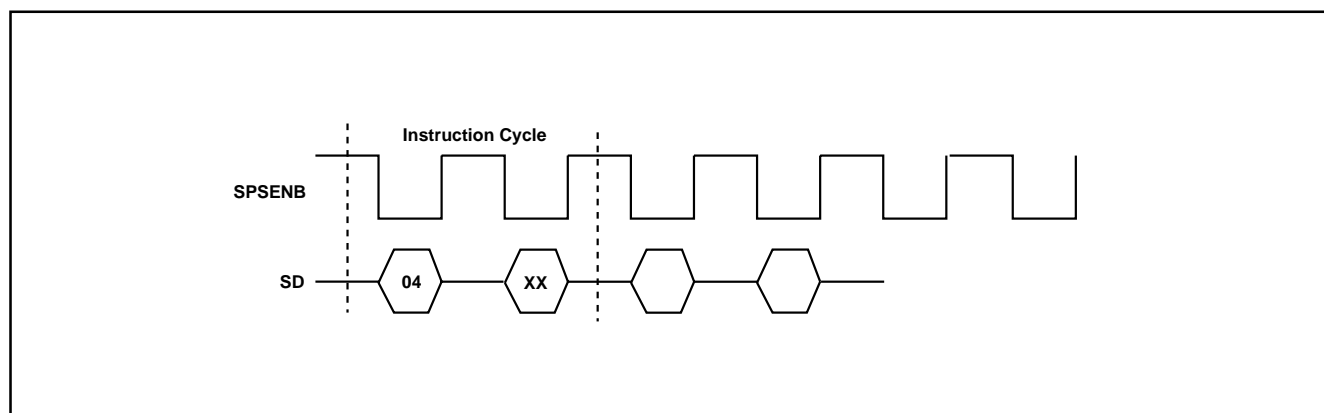


Fig.3 Single Byte Instruction



HEADQUARTERS OPERATIONS
MITEL SEMICONDUCTOR
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (01793) 518000
Fax: (01793) 518411

MITEL SEMICONDUCTOR
1500 Green Hills Road,
Scotts Valley, California 95066-4922
United States of America.
Tel (408) 438 2900
Fax: (408) 438 5576/6231

Internet: <http://www.gpsemi.com>

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- **FRANCE & BENELUX** Les Ulis Cedex Tel: (1) 69 18 90 00 Fax : (1) 64 46 06 07
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- **NORTH AMERICA** Scotts Valley, USA Tel: (408) 438 2900 Fax: (408) 438 5576/6231
- **SOUTH EAST ASIA** Singapore Tel:(65) 3827708 Fax: (65) 3828872
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- **UK, EIRE, DENMARK, FINLAND & NORWAY**
Swindon Tel: (01793) 726666 Fax : (01793) 518582

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